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09/472,869	12/28/1999	Tae-Yong Sohn	Q57124	9316

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EXAMINER
NATNAEL, PAULOS M

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 07/30/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/472,869	SOHN, TAE-YONG	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-9 and 11* is/are allowed.

6)☒ Claim(s) *1-4 and 10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. The responses under 37 C.F.R. § 1.111 have been fully considered and consequently the rejections based on the two references, Han et al. (6,297,850) and Hwang, (6,097,437), have been withdrawn.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

3. Claims **1-4** and **10** are rejected under 35 U.S.C. 102(e) as being anticipated by **Wu** et al., U.S. Pat. No. 6,108,046.

Considering claim **1**, Wu et al. discloses all claimed subject matter, note;

a) the claimed first phase locked loop is met by items 216, 224, 226,222, [PLL 1] FIG. 2; (see col. 5, lines 12-60)

b) the claimed second phase locked loop is by items 218,232,234,236, [PLL 2] FIG. 2; (see col. 5, lines 12-60)

c) the claimed **switching portion for selecting a clock frequency** from one of the first and second phase locked loops according to a predetermined control signal is met by MUX 228, (FIG.2) which selects either the output of VCXO 226 or VCXO 236 outputting 74.25 MHZ or 74.175 MHZ clock.

d) the claimed controller for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of an input digital signal is met by the **Digital Logic Function**, 120 (FIG. 2) which receives an input from the frame rate Detector 135, (FIG. 2), and "provides an output signal 60/59_SEL, that is used by the MUX 228 to select a video sample clock from either the VCXO 226, running at 74.75 MHZ, or the VCXO 236, running at 74.175 MHZ." (See col. 5, line 60 through col. 6, line 5)

Considering claim **2**, the claimed wherein the first phase locked loop generates a clock frequency of 74.25 MHZ, and wherein the second phase locked loop generates a clock frequency of 74.175 MHZ is met by PLLs 1 and 2, FIG.2; (see also rejection of claim 1 (a) and (b))

Considering claim **3,** the claimed wherein the input digital signal has a frame rate selected from the group consisting of 60 Hz, 59.94 Hz, 30 Hz, 29.97 Hz, 24 H z and 23.97 H z, wherein if the frame rate of the input digital signal is one of 60 Hz, 30 Hz and 24 Hz, the controller controls the switching portion to select and output the clock frequency of the first phase locked loop, and wherein if the frame rate of the input digital signal is one of 59.94 Hz, 29.97 Hz and 23.97 Hz, the controller controls the switching portion to select the clock frequency from the second phase locked loop is met by the disclosure that "The SAV/EAV detector and Sample Counter 135 detects the frame rate of the input video signal, e.g., 23.98, 24, 29.97, 30, 59.94, or 60 frames pers second." (Col. 4, lines 28-48, and see also rejection of claim 1 (d)).

Considering claim **4**, the claimed wherein the first phase locked loop generates a clock frequency of 74.25 MHZ, and wherein the second phase locked loop generates a clock frequency of 74.175 MHZ.

Regarding claim **4,** see rejection of claim **2.**

Considering claim **10**, Wu et al. discloses all claimed subject matter, note;

a) the claimed method of receiving said input broadcast signal into said digital signal receiver is met by the input video signal, FIG.1;

B) the claimed method of detecting a frame rate of the input broadcast signal received is met by SAV/EAV detector 100, which detects "a frame rate of the input video signal, e.g., 23.98, 24, 29.97, 30, 59.94, or 60 frames pers second." (Col. 4, lines 28-30)

c) the claimed method of selecting a clock frequency that corresponds to the frame rate which is detected is met by auxiliary Clock 110 and clock rate detector 115 (FIG.1), which includes several multiplexers (FIG.2) that selectively outputs either a clock signal of 74.25 MHZ or 74.175 MHZ according to the TCXO_SEL signal from Micro controller 130.

d) the claimed method of outputting the clock frequency which is selected to components of the digital signal receiver that use the clock frequency to decode and display said input broadcast signal is met by the CLK_54M and CLK_74M output from the master clock generator and clock rate detector, respectively (FIG. 1), and CLK_74M & CLK_54M output from MUX 228 and VCXO 256, respectively, FIG.2.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are

such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim **1** is rejected under 35 U.S.C. 103(a) as being unpatentable over Hatano et al., U.S. Pat. No. 5,933,196.

Considering claim **1**, Hatano discloses the following claimed subject matter, note;

a) the claimed first phase locked loop is met by PLL 62, FIG. 9;

b) the claimed second phase locked loop is by PLL 63, FIG. 9;

Except for;

c) the claimed switching portion for selecting a clock frequency from one of the first and second phase locked loops according to a predetermined control signal; and,

d) the claimed controller for controlling the switching portion to select and output the clock frequency corresponding to a frame rate of an input digital signal.

Regarding c), Hatano does not specifically disclose a switching portion. However, a switching method or apparatus would have to be included in the Scanning line converter 64 in order to switch between CK1 and CK2 output signals of PLL 62 and PLL 63, respectively, for, otherwise the system would have no way of selecting between the two PLL output signals, and the system would fail to function properly.

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to modify the reference of Hatano by adding a selector, a multiplexer, or a switch to selectively switch the output of the two PLL circuits.

Regarding d), although Hatano does not include a control circuit in FIG. 9, Hatano discloses several control circuits in FIGs. 17-20, and since some sort of control mechanism would have to be utilized (otherwise the system would not function properly), it would have been obvious for those skilled in the art to add one of the control circuits disclosed by Hatano and modify FIG. 9 (thus the system of Hatano) in order to control the pixel conversion apparatus in FIG. 9.

6. Claims **2-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hatano et al.**, U.S. Pat. No. 5,933,196 in view of **Wu** et al., U.S. Pat. No. 6,108,046.

Considering claim **2**, the claimed wherein the first phase locked loop generates a clock frequency of 74.25 MHZ, and wherein the second phase locked loop generates a clock frequency of 74.175 MHZ.

Regarding claim 2, Hatano discloses that the clock frequency "has a wide range from about 20 MHZ to over 100 MHZ."

Wu et al., discloses an automatic detection of HDTV video format in which Wu discloses a clock output of 74.25 MHZ or 74.175 MHZ from the Clock rate Detector 115, FIG.1.

Therefore, it would have been obvious to the skilled in the art at the time the invention was made to replace the clock generated in the Hatano system by the teaching of Wu in order to provide a desired clock frequency of 74.25 MHZ and/or 74.175 MHZ, and modify the reference of Hatano.

Considering claim **3,** the claimed wherein the input digital signal has a frame rate selected from the group consisting of 60 Hz, 59.94 Hz, 30 Hz, 29.97 Hz, 24 H z and 23.97 H z, wherein if the frame rate of the input digital signal is one of 60 Hz, 30 Hz and 24 Hz, the controller controls the switching portion to select and output the clock frequency of the first phase locked loop, and wherein if the frame rate of the input digital signal is one of 59.94 Hz, 29.97 Hz and 23.97 Hz, the controller controls the switching portion to select the clock frequency from the second phase locked loop.

Regarding claim 3, Hatano doesn't specifically disclose frame rates. However, Examiner takes an Official Notice in that it is well known in the art that video frame rates such 60 Hz, 59.94 Hz, 30 Hz, 29.97 Hz, 24 H z and 23.97 Hz are used in the tv video signals, and therefore, would have been obvious for those skilled in the art at the time the invention was made.

Considering claim **4**, the claimed wherein the first phase locked loop generates a clock frequency of 74.25 MHZ, and wherein the second phase locked loop generates a clock frequency of 74.175 MHZ.

Regarding claim **4,** see rejection of claim **2.**

Allowable Subject Matter

7. Claims 5-9 and 11 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a digital signal receiver comprising, a video decoder for decoding a video component of a received digital signal into a first input digital signal; an analog to digital converter for converting a received analog video signal into a second input digital signal; a format converter for receiving either of a first and or a second input digital signals, according to which of said first and second input digital signals is present, the format converter converting the input digital signal into a predetermined display format output signal; a controller for detecting the frame rate of the input digital signal received by the format converter and outputting a timing control signal corresponding to the frame rate detected; a clock frequency providing means for providing a clock frequency according to the timing control signal output by the controller, said clock frequency provided to the format converter for converting the input digital signal received by said format converter into said predetermined display output signal; the clock frequency also

provided to said video decoder when said second input digital signal is not present at said format converter, as in claim 5.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tsuchida, U.S. Pat. No. 5,627,598 discloses a display apparatus including aspect ration converter and child picture processing with a four field sequence memory.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Paulos Natnael** whose telephone number is **(703) 305-0019.** The examiner can normally be reached on **Monday through Friday** from **6:30 a.m.** to **3:00 p.m.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **John Miller,** can be reached on **(703)305-4795.**

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is **(703)305-3900.**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communications intended for entry)

or:

(703)872-9314 (for informal or draft communications, please label "PROPOSED" OR "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, V.A. Sixth Floor (Receptionist).

Paulos M. Natnael

July 4, 2002

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